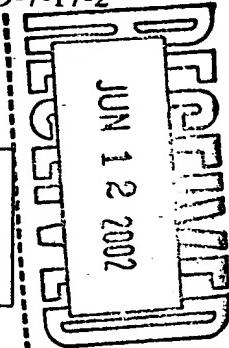




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Diodato 9-7-17-2

6-13-02



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicants(s): Kaxiras et al.  
Case: Diodato 9-7-17-2  
Serial No.: 09/865,847  
Filing Date: May 25, 2001  
Group: 2185  
Examiner: Unassigned

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

Signature:  Date: May 21, 2002

Title: Method and Apparatus for Reducing Leakage Power in a Cache Memory

RECEIVED

INFORMATION DISCLOSURE STATEMENT

JUN 04 2002

Assistant Commissioner of Patents  
Washington, D.C. 20231

Technology Center 2100

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant's attorney wishes to bring to the attention of the Patent and Trademark Office the following documents listed on the accompanying PTO Form 1449. A copy of the listed items are enclosed.

1. Burger et al., "The Declining Effectiveness of Dynamic Caching for General-Purpose Microprocessors," University of Wisconsin-Madison, CS TR #1261, (1995).
2. Powell et al., "Gated-V<sub>dd</sub>: A Circuit Technique to Reduce Leakage in Deep-Submicron Cache Memories," Purdue University, ISLPED '00, Rapallo, Italy, (2000).
3. Wood et al., "A Model for Estimating Trace-Sample Miss Ratios," Proc. of ACM Sigmetrics Conf. on Measurement and Modeling of Computer Systems, (May 1991).
4. Yang et al., "An Integrated Circuit/Architecture Approach to Reducing Leakage in Deep-Submicron High-Performance I-Caches," Proc. of the Seventh Int'l Symposium on High-Performance Computer Architecture (HPCA), (2001).

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability or that no other material information exists.

Respectfully submitted,



Date: May 21, 2002

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Fairfield, CT 06430  
(203) 255-6560

**FORM PTO-1449 (MODIFIED)****LIST OF PUBLICATIONS FOR  
APPLICANT'S INFORMATION  
DISCLOSURE STATEMENT**

Applicant: Kaxiras et al.  
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**COPY OF PAPERS  
ORIGINALLY FILED****U.S. PATENT DOCUMENTS**

EXAMINER	INITIAL	DOCUMENT NO.	DATE	NAME	FILING DATE
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**FOREIGN PATENT DOCUMENTS**

EXAMINER	INITIAL	DOCUMENT NO.	DATE	COUNTRY	TRANSLATION
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**OTHER DOCUMENTS****RECEIVED**

JUN 04 2002

EXAMINER	INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.	CLASS/SUBCLASS	YES	NO
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*Technology Center 2100*

Burger et al., "The Declining Effectiveness of Dynamic Caching for General-Purpose Microprocessors," University of Wisconsin-Madison, CS TR #1261, (1995).

Powell et al., "Gated-V<sub>dd</sub>: A Circuit Technique to Reduce Leakage in Deep-Submicron Cache Memories," Purdue University, ISLPED '00, Rapallo, Italy, (2000).

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Examiner

Date Considered

**Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.